

FIG. 1
PRIOR ART

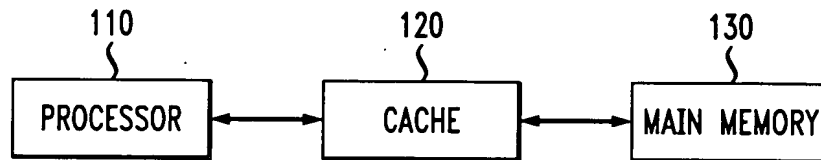


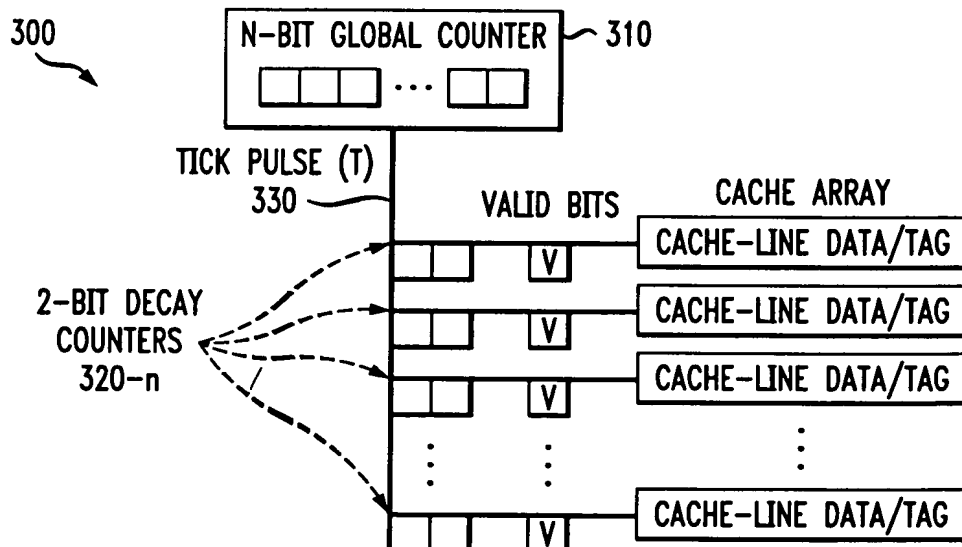
FIG. 2
PRIOR ART

120

CACHE LINE NUMBER	TAG	DATA	VALID BIT
0			
1			
2			
⋮	⋮	⋮	⋮
C-1			

K WORDS

FIG. 3



514

FIG. 4

400

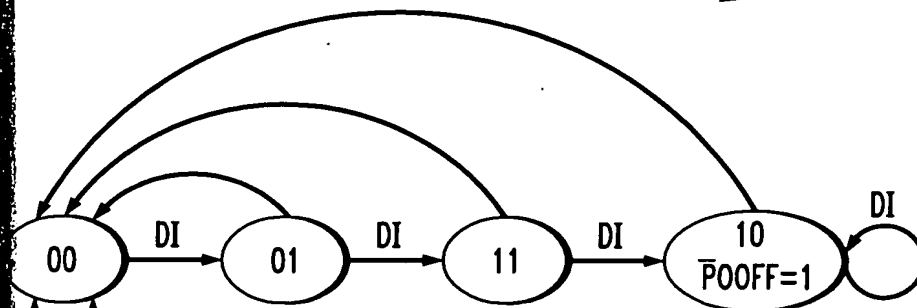
CACHE LINE NUMBER	TAG	DATA	VALID BIT	DECAY INTERVAL 420
0				
1				
2				
⋮	⋮	⋮	⋮	⋮
G-1				

K WORDS

FIG. 8

WRD SIGNAL (ACCESS)

800



$$\text{NEXT } S_0 = S_0 \cdot \overline{\text{DI}} \cdot \overline{\text{WRD}} + \overline{S_1} \cdot \text{DI} \cdot \overline{\text{WRD}}$$

$$\text{NEXT } S_1 = \text{DI} \cdot \overline{\text{WRD}} + S_1 \cdot \overline{S_0} \cdot \overline{\text{WRD}}$$

FIG. 5

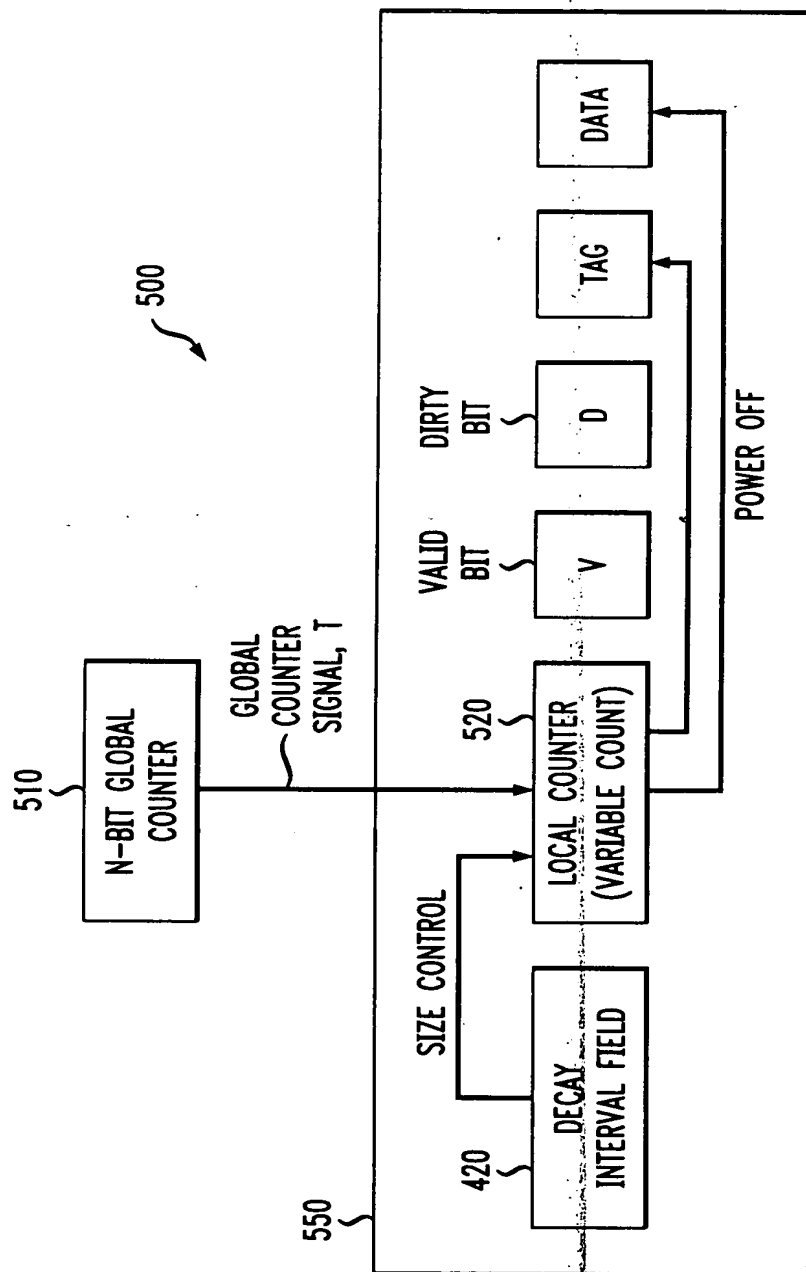


FIG. 6

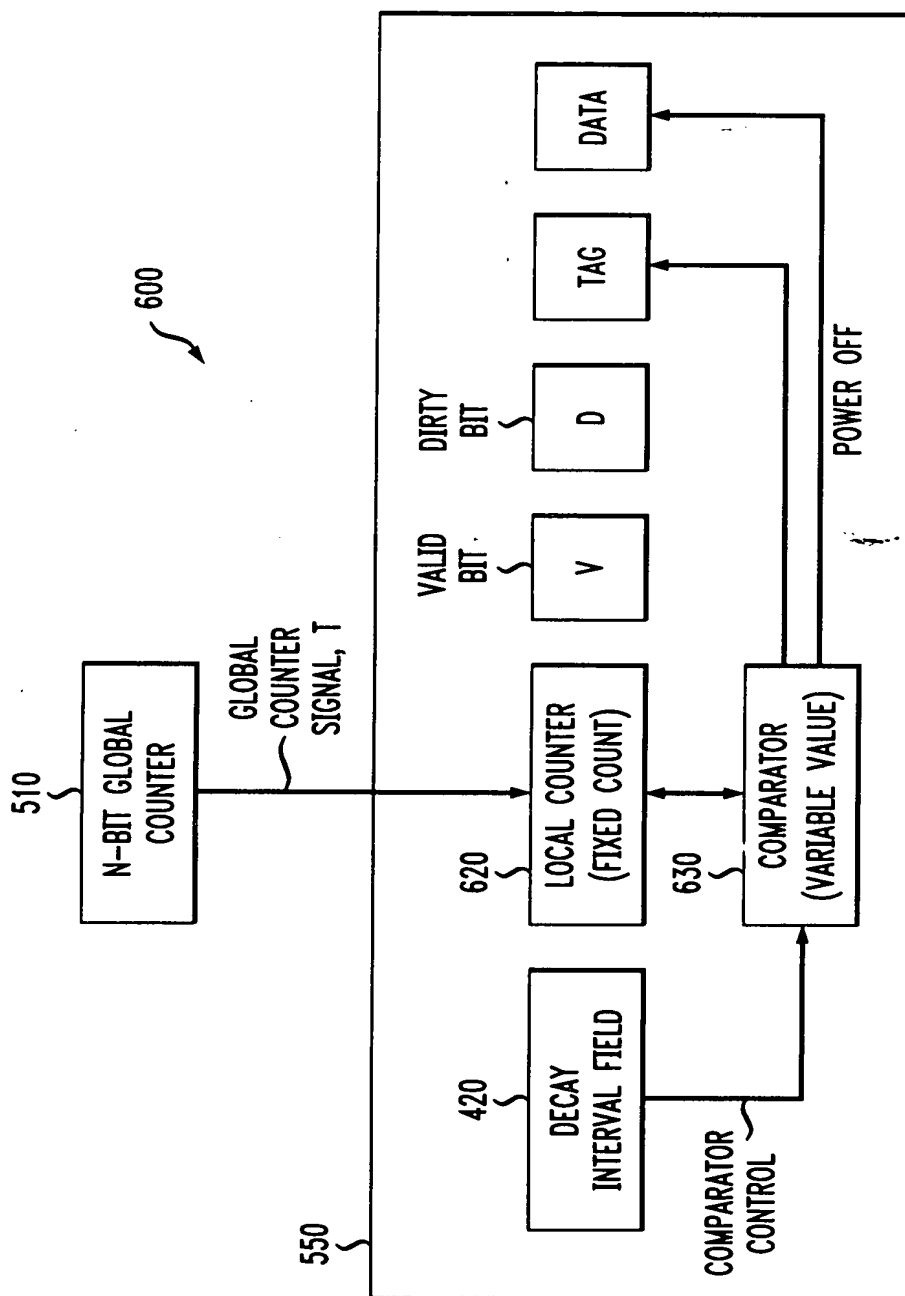


FIG. 7

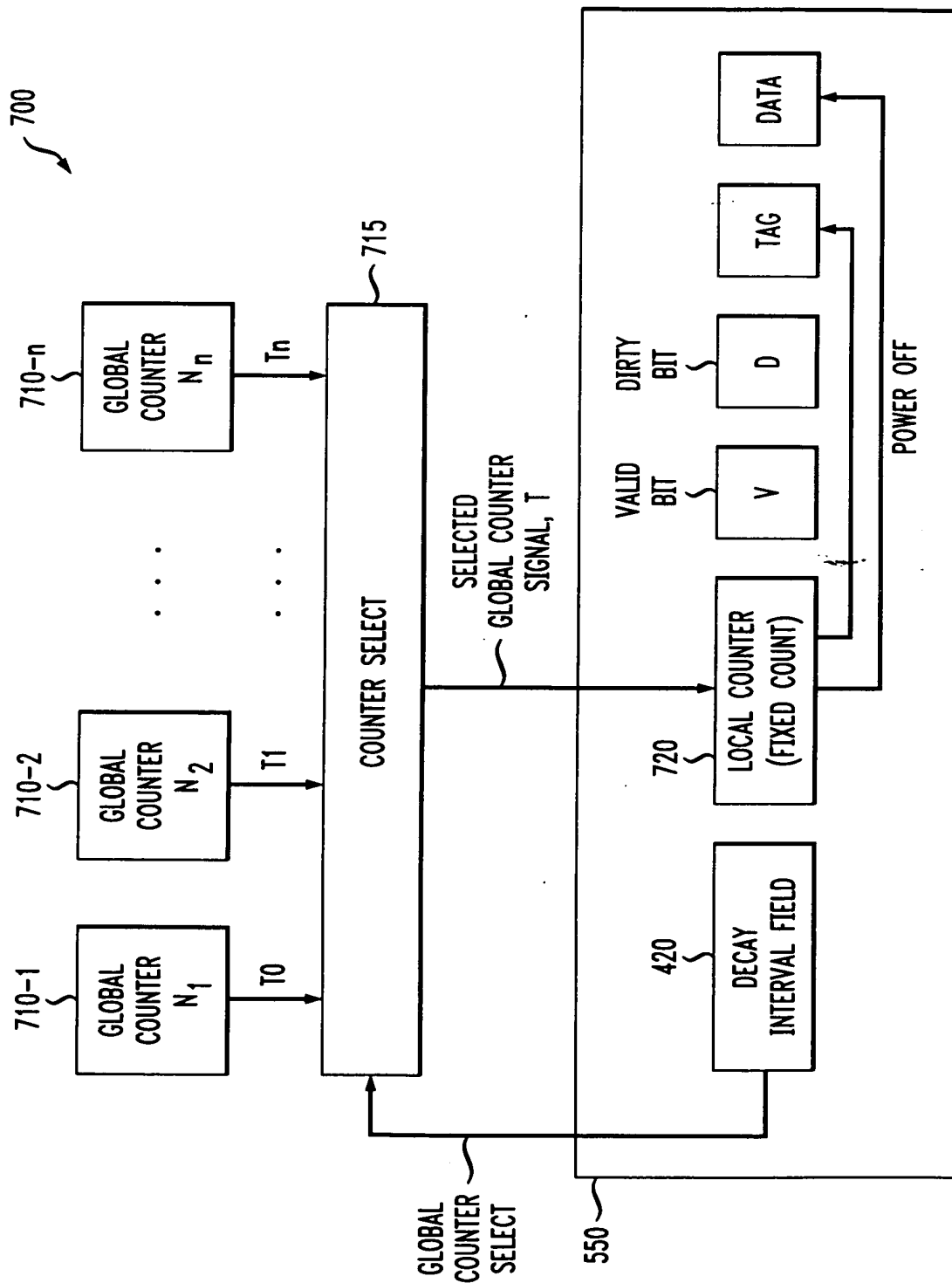


FIG. 9

